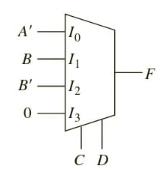
**Project 3**

Develop your VHDL code for the following problems and simulate it is instructed.

Generate one source file for each section of the problem and when you want to simulate a particular one, set it as “top level” using right clock. Submit your project folder and the screen shots for the simulation time diagram.

1. (a) Write a selected signal assignment statement to represent the 4-to-1 MUX shown below.

Assume that there is an inherent delay in the MUX that causes the change in output to occur 10 ns after a change in input.

(b) Repeat (a) using a conditional signal assignment statement.

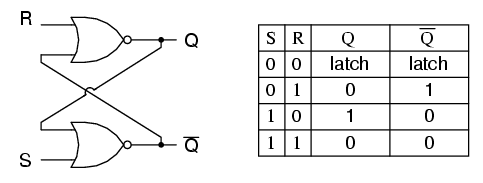
(c) Repeat (a) using a process and a case statement.

* Simulate all cases for when
* A =1, B= 1, C=0, D=0 for 50 ns
* A=1, B=1, C=0, D=1 for 50 ns
* A=1, B=1, C=1, D=0 for 50 ns
* A=1, B=1, C=1, D=1 for 50 ns

1. Write a VHDL description of an SR latch with Q and Q’ outputs

(a) Use a conditional assignment statement.

(b) Use the characteristic equation.

(c) Use logic gates.

* Simulate all cases for
* S= ‘1’, R=’0’ for 50 ns
* S= ‘0’, R=’0’ for 50 ns
* S= ‘0’, R=’1’ for 50 ns
* S= ‘0’, R=’0’ for 50 ns